

ReConFig'05	
Sept. 28, 2005	
8:00 - 9:00	Conference Registration
9:00 - 9:05	Opening Speech
9:05 - 10:45	Session 1 - Architectures <ol style="list-style-type: none"> A Handel-C Implementation of the Back-Propagation Algorithm on Field Programmable Gate Arrays Vijay Pandya, Shawk Alreibi and Medhat Moussa Rapid Prototyping of a Self-Timed ALU with FPGAs Ortega-Cisneros S., Raygoza-Panduro J.J., Suardiaz Muro J., Boemo E. An FPGA-based Parallel Sorting Architecture for the Burrows Wheeler Transform José Martínez, René Cumplido, Claudia Feregino Design and Implementation of an Embedded Microprocessor Compatible With IL Language in Accordance to the Norm IEC 61131-3 Snaider Carrillo L., Agenor Polo Z., Mario Esmeral P.
10:45 - 11:00	Coffee Break
11:00 - 12:00	Talk 1 <i>Vision Sensors using FPGAs</i> Gerardo Sosa, National Institute for Astrophysics, Optics and Electronics
12:00 - 12:15	Coffee Break
12:15 - 14:00	Session 2 - Architectures and Image Processing <ol style="list-style-type: none"> Real-Time FPGA-Based Architecture for Bicubic Interpolation: An Application for Digital Image Scaling Marco Aurelio Nuño-Maganda, Miguel-O Arias-Estrada An Image Comparison Circuit Design Miguel Angel Sánchez Martínez and Adriano De Luca Pennacchia FPGA-Based Customizable Systolic Architecture for Image Processing Applications Griselda Saldaña, Miguel Arias-Estrada FPGA implementation of a synchronous and self-timed neuroprocessor Raygoza-Panduro J.J., Ortega-Cisneros S., Boemo E.
14:00 - 16:00	Lunch break
16:00 - 17:40	Session 3 - Arithmetic <ol style="list-style-type: none"> An FPGA Arithmetic Logic Unit for Computing Scalar Multiplication using the Half-and-Add Method Sabel Hernández-Rodríguez, Francisco Rodríguez-Henríquez Hardware signal processing unit for one-dimensional variable-length discrete wavelet transform Ordaz-Moreno Alejandro, Romero-Troncoso Rene de Jesus, Vite-Frias Jose Alberto VHDL Core for 1024-Point Radix-4 FFT Computation Vite-Frias Jose Alberto, Romero-Troncoso Rene de Jesus, Ordaz-Moreno Alejandro FPGA Implementation of an efficient multiplier over finite fields GF(2^m) Mario Alberto García-Martínez, Rubén Posada-Gómez, Guillermo Morales-Luna, Francisco Rodríguez-Henríquez
17:40 - 18:00	Coffee Break
18:00 - 19:00	Keynote Speech 1 <i>Reconciling Logic and Objects</i> Robert Kowalski, Imperial College, UK
19:00 - 20:00	Official Opening
20:00 - 21:00	Toast and Cultural Event

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Sept. 29, 2005	
8:00 - 9:00	Conference Registration
9:00 - 9:05	Welcome Day 2
9:05 - 10:45	Session 4 - Reconfiguration <ol style="list-style-type: none"> On the Design of Two-Level Reconfigurable Architectures Sebastian Lange, Martin Middendorf A Secure Self-Reconfiguring Architecture based on Open Source Hardware Javier Castillo, Pablo Huerta, José Ignacio Martínez Platform for Intrinsic Evolution of Analogue Neural Networks Patrick Roche, John Maher, Fearghal Morgan Dynamic Voting Schemes to Enhance Evolutionary Repair in Reconfigurable Logic Devices Corey J. Milliard, C. A. Sharma, R. F. DeMara
10:45 - 11:00	Coffee Break
11:00 - 12:00	Keynote Speech 2 <i>High Performance Computing using Reconfigurable Hardware</i> Viktor K. Prasanna, University of Southern California,
12:00 - 12:15	Coffee Break
12:15 - 14:00	Session 5 - Physical Design <ol style="list-style-type: none"> Design Space Exploration of Coarse-Grain Reconfigurable DSPs Martin Zabel, Steffen Köhler, Martin Zimmerling, Thomas B. Preußner, Rainer G. Spallek Optimizing Register Binding in FPGAs Using Simulated Annealing Annie Avakian, Iyad Ouass Hierarchical FPGA clustering based on a multilevel partitioning approach to improve routability and reduce power dissipation Zied Marrakchi, Hayder Mrabet, Habib Mehrez A novel FPGA Implementation of a Welding Control using a new Bus Architecture Rauma K., Luukko J., Härkönen T., Pajari, I. and Pyrhönen O.
14:00 - 16:00	Lunch break
16:00 - 17:40	Session 6 - Tools <ol style="list-style-type: none"> High quality uniform random number generation for massively parallel simulations in FPGAs David Thomas, Wayne Luk VANNGen: a Flexible CAD Tool for Hardware Implementation of Artificial Neural Networks André Braga, Carlos Humberto Llanos, Mauricio Ayala-Rincón, Ricardo P. Jacobi Quartz: A Framework for Correct and Efficient Reconfigurable Design Oliver Pell, Wayne Luk Applied VHDL Training Methodology, EDA Framework and Hardware Implementation Platform Fearghal Morgan, Patrick Roche, Martin O'Halloran
17:40 - 18:00	Coffee Break
18:00 - 19:00	Keynote Speech 3 <i>Model Construction of Nonrigid Biological Objects from Images</i> Dmitry Goldgof, University of South Florida
20:30	Dinner

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Sept. 30, 2005	
9:00 - 9:05	Welcome Day 3
9:05 - 10:45	Session 7 - Signal Processing <ol style="list-style-type: none"> On the design of an FPGA-Based OFDM modulator for IEEE 802.16-2004 Joaquin Garcia, Rene Cumplido FPGA Implementation of DSVPMW Modulator Ossi Laakkonen, Hannu Sarén, Kimmo Rauma, Olli Pyrhönen An FPGA-based Coprocessor for the SPHINX Speech Recognition System: Early Experiences Guillermo Marcus, Juan A. Nolasco-Flores Hardware/Software implementation of a Discrete Cosine Transform Algorithm Using SystemC A. Avila, R. Santoyo, S. O. Martinez, G. Dieck
10:45 - 11:00	Coffee Break
11:00 - 12:00	Keynote Speech 4 <i>Topic TBA</i> Alexander Gelbuck, IPN Mexico
12:00 - 12:15	ReConFig Closing Toast and Awards

NOTE: Keynote Speeches are common to ReConFig and ENC. They will be open to attendees of both conferences.